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A 1V Phase Frequency Detector (PFD) with 180nm CMOS Technology

N. K. Kaphungkui
Dept. of ECE, Dibrugarh University, Assam, India
Corresponding Author: pipizs.kaps@gmail.com

***Abstract* — In this paper, designing of a Phase frequency detector with 180nm CMOS technology is presented. The main objective of the designed circuit is to reduce the power dissipation with a low voltage supply of 1V. Phase frequency detector has a wide range of applications but one of the main application is in modern day phased locked loop, it serve as a main building block. PFD (Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, and has two outputs UP and DOWN which are signalled according to the phase and frequency difference of the two input signals. The designed circuit shows a satisfactory result with the low supply voltage. The detection of phase difference occurs only at the rising edge of the two clock signal. The total power dissipation from the circuit is only 3.88uW which is considerably low. In the field of IC design power dissipation of the circuit is always an important factor. The lower the power dissipation the longer the service time of the battery powered electronics circuit.**

***Keywords* – Phase Locked Loop, Phase Frequency Detector, Phase Error, VCO.**

I. INTRODUCTION

A phase locked loop (PLL) is a feedback system that includes a voltage control oscillator (VCO), phase frequency detector (PFD), and a charge pump. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when it is locked. PLLs have been widely used in high performance microprocessors and high speed digital communication systems as clock generator. Many works has been presented in designing PLL by different groups worldwide having different power dissipation. This paper described one of the basic building blocks of PLL, i.e. phase frequency detector with much lower power dissipation which can work efficiently with 1V using 180nm CMOS technology. References [2] and [3] are reported for higher frequency range with higher supply voltage of 1.8V and higher power consumption.
Here the main objective of this paper is to operate at lower frequency range with lower voltage supply and power. The circuit detect the phase difference only at the rising edge of the clock cycle.

II. PHASE FREQUENCY DETECTOR

Phase Detector (PD) can be implemented by XOR (exclusive OR) logic gate. The simple operation of exclusive OR gate is, it compare phase difference between both signal and produces output pulses depending upon the input variation. The working principle of PD is similar to that of differential amplifier. In both the case it senses the difference between the inputs and generates a proportional output. One property of XOR gate is it detects the phase difference during both the rising edge and falling edge of clock cycle. Implementation and simulation result with different phase difference between reference and feedback signals of XOR phase detector in sub nanometre CMOS technology is already presented along with their characteristics [4]. Another class of digital phase detector and the most common which is use in PLL is phase frequency detector (PFD). This type detects both the phase and frequency difference between two signals. Simplified block is given in fig 1

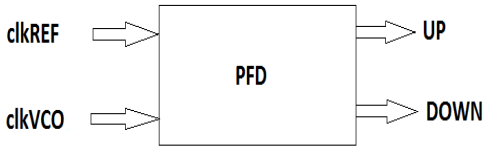

Fig.1. Block diagram of a Phase frequency detector

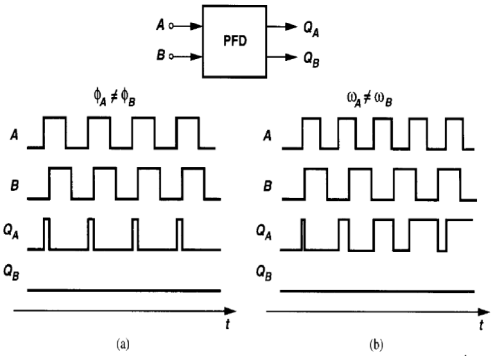

Fig.2. PFD output according to the two input conditions

With reference to [1] the basic working principle of phase frequency detector is described briefly as follow. From fig2 If initially $Q_A = Q_B = 0$, then the rising transition on A leads to $Q_A = 1$, $Q_B = 0$. The circuit remains in this state until B goes high, at which point Q_A returns to zero. The behaviour is same for the B input. In the figure2.(a) the two inputs have equal frequencies but A leads B. The output Q_A continues to produce pulses whose width is proportional to Q_A - Q_B while Q_B remains at zero. In the figure2 (b) A has a higher frequency than B and Q_A generates pulses while Q_B does not. By symmetry, if A lags B or has a lower frequency than B, then Q_B produces pulses and Q_A remains quite. Thus, the dc contents of Q_A and Q_B provide information about $\varphi_A - \varphi_B$ or ω_A - ω_A. The outputs Q_A and Q_B are called the UP and DOWN pulses respectively. When both A and B have the same frequency and phase then only Q_A and Q_B will remain in zero state. This is the condition with no phase error. The input phase difference of the two signals and the average output

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voltage is shown in fig4. The more the phase difference between the two signals, the more the average output voltage up to a phase difference of $\pi_{/2}$. The output is linear with phase difference between the two signals. After phase difference $\pi_{/2}$ the average output decrease linearly again and finally becomes zero at 2π.

III. Circuit and Simulation Result

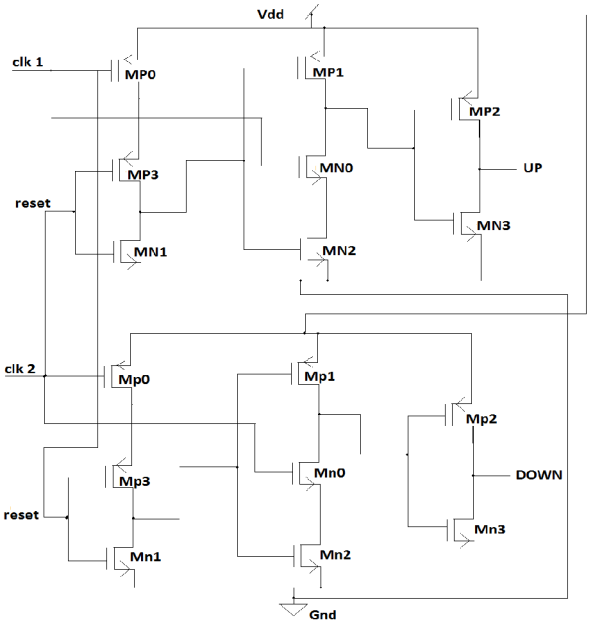

Fig.3. Circuit diagram of PFD

Fig.3 shows the circuit implementation of Phase Frequency Detector requiring 16 MOS with 180nm CMOS technology. Simulation timing diagram as shown in this section is carried out at 100 MHz with both the clock signal having a rise time and fall time of 1ps each with 50% duty cycle and amplitude of 1V. The circuit performed best from 125 KHz range up to as high as 500MHz. The length and width of the MOS is optimised precisely such that the simulation result is almost ideal with no error. The total power dissipation of the circuit is 3.88uW.The various simulation result waveform is included in this section for different input condition.
The input/output characteristic of the PFD is shown below in Fig.4.

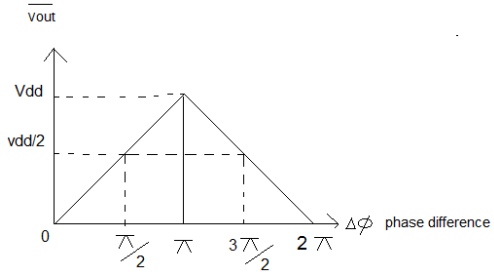

Fig.4. Input/output characteristic

When clk2 is leading the clk1 by 25ns (nanosecond) i.e. $\pi_{/2}$ the down pulse goes high as shown in the simulation result below in Fig.5

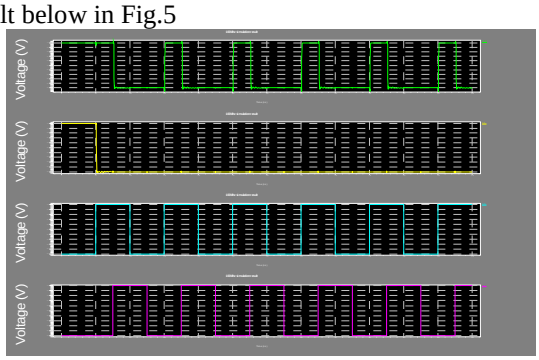

Fig.5. The down pulse goes high when clk2 is leading

Similarly when clk2 is lagging the clk1 by the same time delay or phase delay the up pulse goes high.

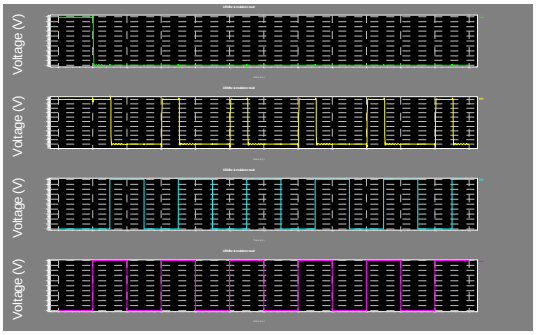

Fig.6. The up pulse goes high when clk1 is leading

But when both the clocks have the same phase and frequency i.e. zero phase difference or 2π then the output pulses UP and DOWN remains in the zero state. From the simulation result there is no phase error as shown below.

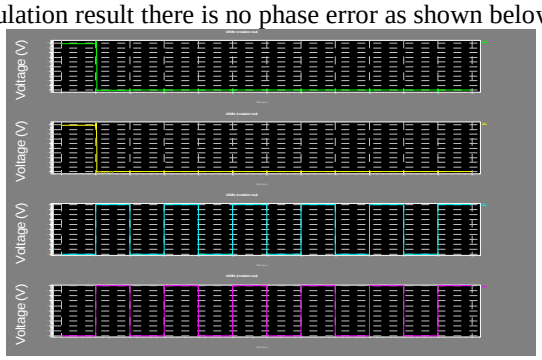

Fig.7. No phase error simulation result when both the clock are of same frequency and phase

IV. Design Result

operating freq range	upto 500 MHz
circuit current	3.88 uA
total power dissipation	3.88 uW
supply voltage	1 V
technology used	CMOS 180nm
zero phase error	no error at output

V. CONCLUSION

This phase frequency detector is implemented with 16 transistors at 180nm CMOS technology with a low supply of 1V. Circuit power dissipation mainly depends upon the supply voltage. By lowering the supply voltage and scaling the length and width of the CMOS at the appropriate proportion, the total circuit power dissipation is lowered without affecting the circuit performance. In section IV all the simulation satisfactory results are shown. Properly scaling the gate size, threshold voltage of the MOS transistor can be still lowered and hence it can operate with a supply voltage as low as 1V. Reducing the chip size increase the speed of operation on the other hand. The tool use for the simulation is TANNER and at 180 nm technology.

REFERENCES

[1] B.Razavi, "Design of Analog Cmos Intrgrated Circuit",TATA McGraw Hill Publisher.

[2] S. B. Rashmi, Siva S. Yellampalli "Design of Phase Frequency Detector and Charge Pump for High Frequency PLL" International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-2, Issue-2, May 2012

[3] Dr. K.B.Khanchandani, Chandan Kumar Akela " Designing of Phase Frequency Detector for High Speed Applications of Phase Locked Loop (PLL)" *Published in International Journal of Advanced Engineering & Application, Jan 2011Issue*

[4] Delvadiya Harikrushna I1, Prof. Mukesh Tiwari2, Prof. Jay Karan Singh3, Dr. Anubhuti Khare4" Design, Implementation And Characterization Of XOR Phase Detector for DPLL in 45 NM CMOS Technology" Advanced Computing: An International Journal (ACIJ), Vol.2, No.6, November 2011.

[5] Kang, Sung-Mo & Leblebici Yusuf. CMOS Digital Integrated Circuits. New York: McGraw-Hill, 2003.

[6] HenrikO.Johansson,"ASimple Precharged CMOS Phase Frequeny Detector" IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL.33, NO.2, FEBRUARY 1998.

[7] Kang, Sung-Mo & Leblebici Yusuf. CMOS Digital Integrated Circuits. New York: McGraw-Hill, 2003

AUTHOR'S PROFILE

N. K. Kaphungkui

Completed Diploma in Electronics Engineering in the year 2004 from DOEACC centre and after that received B.Tech. Degree in Electronics and Communication in the year 2007 from North East Regional Institute of Science and Technology. And pursue M.Tech in Electronics Design and Technology in 2009 and completed in the year 2011 from Tezpur University. Presently working as faculty member in Dibrugarh University, Assam, India. Area of research interest includes VLSI design, simulation and circuit analysis and implementing with CMOS device.
Email ID: pipizs.kaps@gmail.com.